The development of a real-time Monitoring system for the ATLAS Tile Calorimeter Phase-II Upgrades

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Abstract. A major upgrade to the High Luminosity Large Hardon Collider (LHC) will increase the instantaneous luminosity by a factor 5 compared to the LHC. A complete redesign of the electronic system is required for new radiation levels, data bandwidth as well as the clock distribution. This new design is called the A Toroidal LHC ApparatuS (ATLAS) Tile Calorimeter (TileCal) Phase-II upgrade system. This is an integration of the front-end and back-end electronics to meet technical requirements of the design. Numerous sensors will be used to monitor the status of the ATLAS TileCal Phase-II upgrade system. This paper presents a real-time monitoring system that will be used to read data from the sensors of the TileCal electronic system that will be used by the Detector Control System (DCS). The real-time monitoring system includes an implementation of a server on the System-on-Chip (SoC) Zynq Field Programmable Gate Array known as Tile Computer-on-Module (TileCoM). This server will read data and publish it to the clients of the DCS. A test bench that includes an Avnet Ultra96-V2 ZYNQ UltraScale+ MPSoC evaluation board and Tile Gigabit Ethernet switch that serves as a basis for the TileCoM mezzanine board as part of the Tile PreProcessor (TilePPr).

1. Introduction

For the discovery of the Higgs boson, the Large Hadron Collider (LHC) [1] collide protons at a centre of mass energy of 14 TeV with a luminosity of $1 \times 10^{-34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$. The LHC is upgraded to the High-Luminosity Large Hadron Collider (HL-LHC) [2] to reach an instantaneous luminosity of $7.5 \times 10^{-34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$. The HL-LHC will produce about 200 proton to proton collisions per bunch crossing at an integrated luminosity (3000–4000 fb^{-1}). ATLAS is one of the four experiments for the HL-LHC. The basic principle of this experiment involves the collision between two proton beams at the center of the ATLAS detector generating particles in all directions. To detect the ionising radiation, the Pixel detector and the semiconductor tractor (SCT) utilizes silicon and microstrips. The trajectories of the charged particles are bent by the magnetic field produced from Inner Detector. Figure 1 shows the ATLAS detector which is a general-purpose particle detector for the LHC [3]. The Tile Calorimeter (TileCal) [4] is a sampling calorimeter with steel as an absorber and scintillator tiles as active medium. The TileCal detector is divided into a long inner barrel and two extended barrels on both sides of the

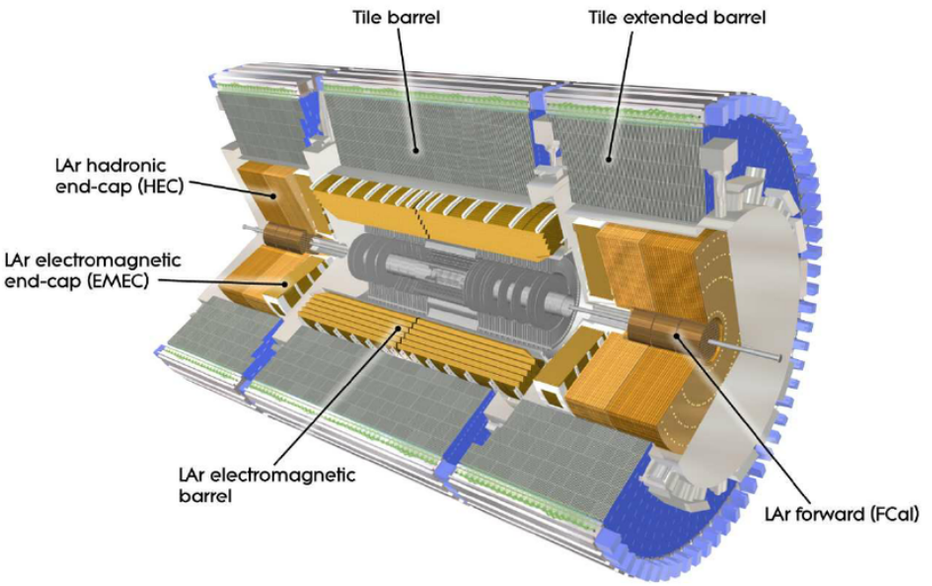

Figure 1. *The ATLAS detector* [3].

detector. Due to the new requirements of the HL-LHC, the ATLAS TileCal Phase II upgrades redesign the ATLAS TileCal readout electronic chain. The TileCal detector modules consists of the wavelength-shifting (WLS), scintillators and the photomultiplier tubes (PMT). The On-detector electronics takes snapshots of the ultraviolet scintillation light in nano seconds (ns) using Photo-Multipliers (PMT). These PMT signals are digitized by Front-End (FE) electronics, serialized and sent to the Back-End (BE) electronics. This is a project in instrumentation for particle physics.

2. The Atlas Tile Calorimeter Phase II Upgrade

Figure 2 shows the proposed redesign of the electronic system [5] to read-out data from the detector. The system is divided into FE electronics that are on the detector and BE electronics. The analog signals from the FENICS board are then converted into digital signals by the ADCs on the Main board. The Daughter Board transmits digital data from the FE to the BE through GBT protocol. These data is transmitted at the HL-LHC frequency of 40 Mhz. The BE electronics consists of the TileCal Pre-Processor (TilePPr) [6] that receives digital data and process it in a pipeline memories of the FPGA. The Trigger Data Acquisition Interface (TDAQi) [7][8] communicates with the TilePPr. All the TilePPr electronics are housed inside the Advanced Telecommunication Computing Architecture (ATCA) [9] that can be remotely configured and controlled through the Gigabit Ethernet. The TileCoM is one of the TilePPr modules and it is used for three main functionalities. Section 3 presents one of the main functionalities of TileCoM.

3. The TilePPr-DCS communication system

All the boards that are installed on the ATLAS TileCal Phase II upgrade electronics readout chain have sensor components. These sensor components measures temperature, voltage, current, humidity, etc. A software functionality is implemented to integrate with these sensors to be able to remotely control and monitor the electronic readout chain.

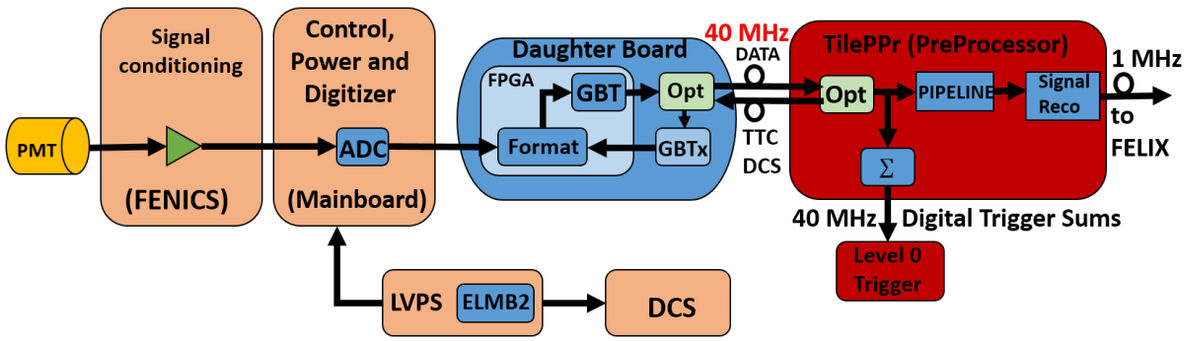

Figure 2. *The ATLAS Tile Calorimeter Phase II Upgrade electronic readout system* [5].

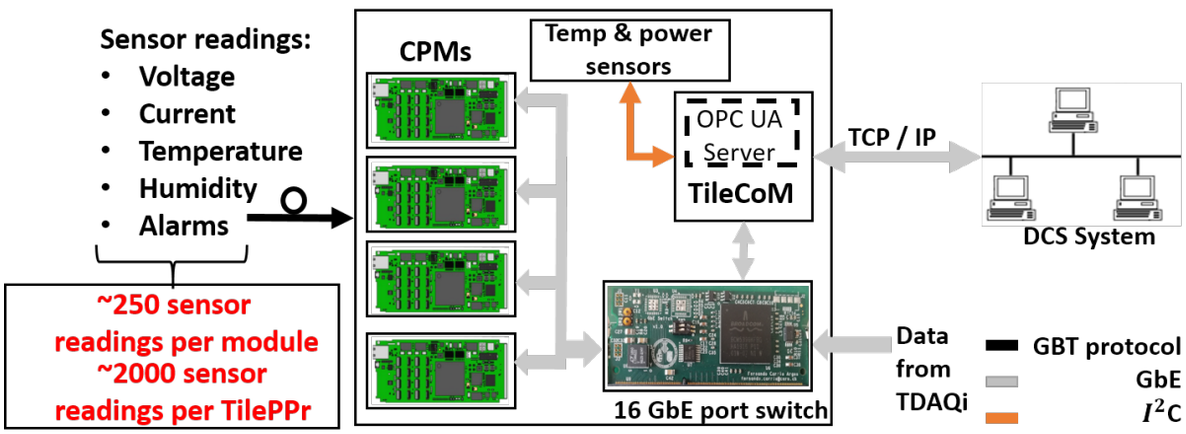

Figure 3. *The ATLAS Tile Calorimeter TilePPr-DCS communication system.*

This functionality is implemented to ensure healthy operation of the electronics at all times. This functionality is implemented in the TileCoM on the BE electronics. Gigabit Ethernet (GbE) and Inter-Integrated Circuit (I^2C) are used as communication protocols between the TileCoM and the BE electronics. Figure 3 shows the general block diagrams of the TilePPr and the DCS [10] interface functionality. This block diagram shows the connection of all the components of the FE and BE electronics. The TilePPr and the DCS interface functionality will read data from approximately 2000 sensors from the FE electronics into the BE electronics. This data from the FE electronics is transferred through the Gigabit Transceiver (GBT) protocol to the BE electronics. In order to implement this functionality and to remotely monitor this data, two server applications are implemented on the TileCoM to readout data sensor data and publishes this data to the DCS client.

These two server applications are implemented using the open source and stable framework called the Quick OPC UA server generation framework (Quasar) framework [11]. This framework is used to efficiently implement OPC UA servers in a short period of time with precise data reading from the sensors. This is achieved by allowing the developer to create design files using XML documents with minimal C++ development. The XML files are also used for configuration purposes in order to publish to the client and to also act as a lightweight data-interchange format between the hardware and the software applications. The first server (OpcUATileXADC) readout XADC sensor data from the TilePPr modules. This server access the low-level ADC device tree, IIO library and the Linux virtual file system to be able to interface with the

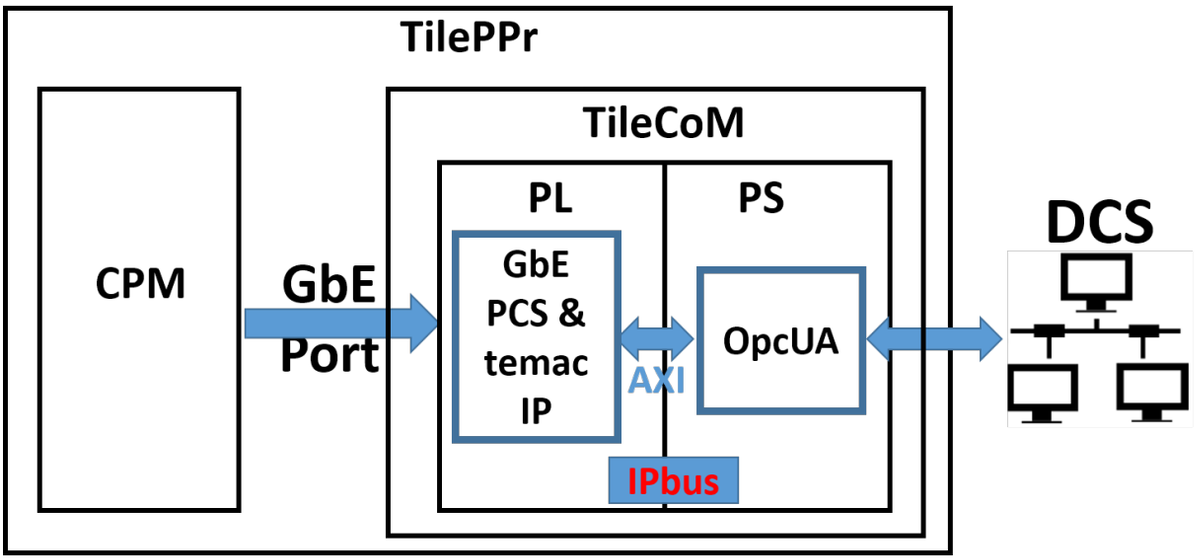

Figure 4. *The second OpcUA server block diagram for the TilePPr-DCS system.*

hardware. When the server is executed on the TileCoM, it reads sensor data and publishes this data to the Supervisory Control and Data Acquisition (SCADA). Figure 4 shows a block diagram of the second server (OpcUATile) block diagram for the TilePPr-DCS system. An IPbus implementation is integrated with the quasar framework to read sensor data. This IPbus is implemented using the Ironman [12] open source framework. The IPbus enables flexible integration and reading of data between the CPM and the TileCoM. This functionality will also be used to read sensor data from the ATCA carrier. For this sensor data acquisition, the server will use the I^2C protocol to interface with the ATCA carrier sensors.

4. The implementation of OpcUA servers for TilePPr-DCS communication system

4.1. Test-bench to readout sensor data from the readout electronic chain

The main objective of this software development and the TileCoM functionality is to remotely control and to monitor the readout electronic chain. Figure 5 shows an integration of the first prototype for the TilePPr-DCS communication system. This test-bench resembles the readout architecture as shown in Figure 3. The CPM emulator board is used to resemble the CPM for the ATLAS TileCal Phase II upgrade readout electronic chain. The computer is used to serially connect the embedded Linux running on the TileCoM. The power supply is used to power the CPM and the TileCal GbE Ethernet Switch motherboard. The Network router enables remote connection to the whole test-bench together with the TileCal GbE Ethernet Switch. The Avnet Ultra96-V2 ZYNQ UltraScale+ MPSoC TileCoM evaluation board is used to run the OpcUaXADC server. The CPM Emulator board is a Xilinx Virtex-7 FPGA VC707 Evaluation Kit that is used for test purposes. This evaluation board implements a similar VHDL firmware code that is used to readout sensor data from the FE electronics. The TileCal GbE Ethernet Switch motherboard has 24 ports to allow as many boards to be connected to the network as possible. These boards are powered with 12V power supply which is the same voltage that will be used for the final design of the BE electronics components.

4.2. Progress results for the OpcUA servers

This contribution is a work in progress of the implementation of OpcUA servers. For this contribution and test purposes, presentation results for the firs server are discussed. Only

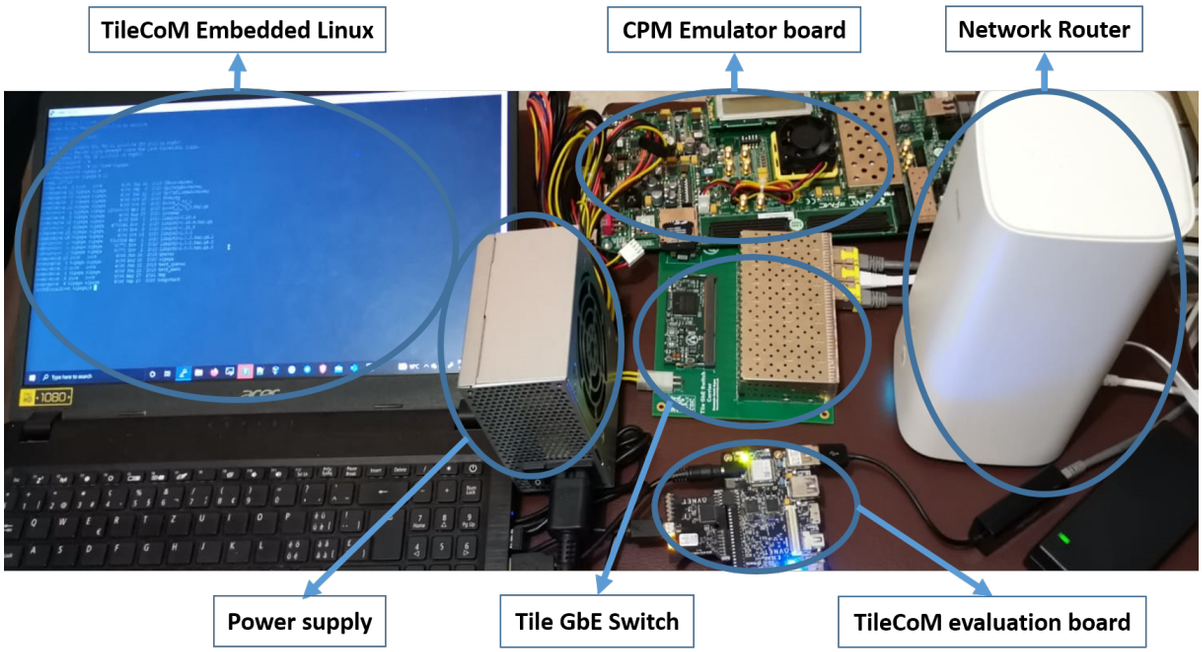

Figure 5. *Server and client communication test-bench.*

voltages and temperatures sensor readings are acquired from the OpcUATileXADC server running on the TileCoM. This server is running on the CentOS embedded Linux shown on the left side of figure 5. An executable is used to run the server on the embedded Linux terminal. Only the XADC values were acquired from the OpcUATileXADC. Figure 6 shows the results for the OpcUATileXADC server. The figure shows the results for the vcc ps batt, Vcc aux, vcc ps ddr, vcc int and vcc bram sensors. The voltage values obtained for each sensor are 2.89 for vcc ps batt, 2.88 for Vcc aux, 1.76 for vcc ps ddr, 1.35 for vcc int and 1.35 for vcc bram sensors. However, according to the datasheet of the TileCoM evaluatiob board used for the test, the results obtained are not exact values. The exact values according to the datasheet [13] are 2.80 for vcc ps batt, 2.80 for Vcc aux, 1.80 for vcc ps ddr, 1.40 for vcc int and 1.40 for vcc bram sensors. Thus, the error analysis between the measured results and the expected results is 0.09 for vcc ps batt, 0.08 for Vcc aux, 0.04 for vcc ps ddr, 0.05 for vcc int and 0.05 for vcc bram sensors.

5. Conclusion

This contribution is based on real-time control and monitoring for the ATLAS Calorimeter Phase-II upgrade electronic system. This is a project in instrumentation for particle physics. It is part of the electronic system for the ATLAS Calorimeter Phase-II upgrade. Two servers are implemented on the TileCoM to connect to read out on- and off-detector electronics. The acquired sensor data is published to the UA expert or SCADA for DCS to monitor the system. This software application is vital for the electronics readout chain to be able to remotely control and monitor all the sensors on the system. As this is the first stage of integration test for the TilePPr-DCS communication system, this functionality is tested using commercial boards for the TileCoM and the CPM to readout XADC sensor data. Results for the first server (OpcUATileXADC) are discussed and the second server (OpcUATile) is a work-in progress.

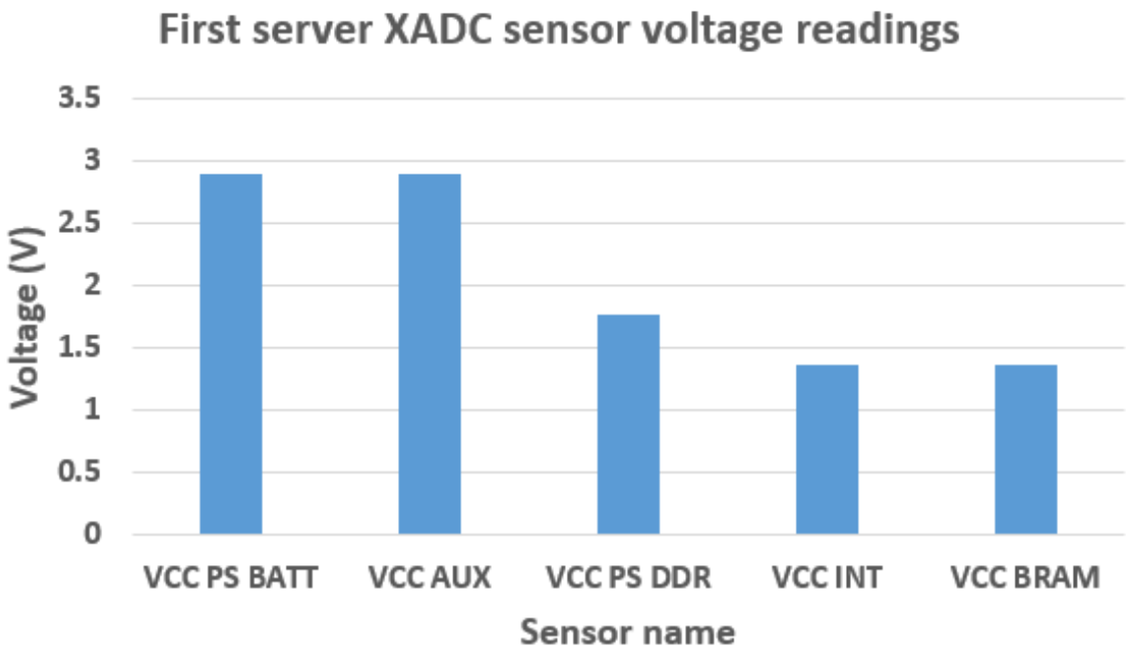

Figure 6. The ATLAS TileCal OpcUA server XADC results.

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